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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,250	SASSER ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8-1-2008; 9-8-2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submissions filed on 01 August 2008 and 08 September 2008 have been entered.

Allowable Subject Matter

2. The indicated allowability of claims is withdrawn in view of the newly discovered reference to Ishizuka et al. (US 5,479,288 A). Rejections based on the newly cited reference (in various combinations with other references) follow. Also, upon further consideration, double patenting rejections are made of claim 53 in view of various patented claims as discussed in detail below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 2, 4, 7, 8, 11, 12, 15-17, 19, 22, 23, 27-31, 35-37, and 47-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** (US 5,019,769 A) in view of **Ishizuka et al.** (US 5,479,288 A).

Regarding **claim 1**, Levinson discloses an optoelectronic module (Figure 3), comprising:

an optoelectronic component (e.g., laser diode 100 or photo diode 224);

a controller IC (including microcontroller 162) including a serial digital interface (i.e., RS232 I/O port 200) configured to facilitate communication, between the optoelectronic module and a host (i.e., computer 202), of diagnostic parameter information concerning the optoelectronic component (column 6, lines 40-59).

Similarly, regarding **claim 17**, Levinson discloses an optical transceiver module (Figure 3), comprising:

a transmit optical subassembly (including laser diode 100);

a receive optical subassembly (including photo diode 224);

a controller IC (including microcontroller 162) including:

a serial digital interface (i.e., RS232 I/O port 200) configured and arranged to facilitate communication, between the optical transceiver module and a host (i.e., computer 202), of diagnostic parameter information relating to at least one of: the transmit optical subassembly; and, the receive optical subassembly; and

a plurality of memory mapped locations (such as locations within memory element 166), at least one of which is configured to store diagnostic parameter information and is accessible by way of the serial digital interface (column 10, lines 28-66; column 15, lines 26-36).

Regarding both claims 1 and 17, Levinson does not specifically disclose positioning the elements of the transceiver system in a housing and does not specifically disclose a pinout arrangement comprising: a pin array having a plurality of pins in communication with the controller and a pair of pins in communication with the interface.

However, it is well understood in the art that a transceiver system such as disclosed by Levinson may be placed in a housing in order to protect the various components from damage. Ishizuka et al. teach a system that is related to the one described by Levinson, including an optical transmitter 201, an optical receiver 202, and controller elements including circuit 203 (Figures 2A-C). Ishizuka et al. further teach disposing the transceiver elements in a housing 405 and further teach a pin array (i.e., lead terminals 404).

Examiner notes that Ishizuka et al. particularly teach that the pins and electrical contacts are used to enable the transceiver components within the housing to further connect to and communicate with additional elements outside of the housing in the context of an overall communication system (column 6, lines 21-32 and column 8, Table 2).

Regarding claims 1 and 17, it would have been obvious to a person of ordinary skill in the art to provide a housing as taught by Ishizuka et al. in the system disclosed by Levinson in order to advantageously protect the optoelectronic elements from damage while enabling the elements to transmit and receiver optical signals and connect to other elements of the communication system. It further would have been obvious to a person of ordinary skill in the art to provide a pin array and pins as taught by Ishizuka et al. in the system disclosed by Levinson in order to advantageously enable the components of the optical transceiver to physically connect to other elements through the housing. Examiner notes that Levinson already discloses that the transceiver includes an interface (RS232 I/O port 200) that is connected to a host computer. In the system described by Levinson in view of Ishizuka et al. as discussed above, it would have been obvious to a person of ordinary skill in the art to provide the interface connection disclosed

by Levinson through pins as taught by Ishizuka et al. in order to enable the interface connection to extend from the protective housing and effectively connect to the host computer.

Regarding **claim 2**, Levinson discloses that the optoelectronic component comprises at least one of: a transmit optical subassembly (i.e., laser diode 100); and, a receive optical subassembly (i.e., photo diode 224).

Regarding **claims 4 and 19**, in the system described by Levinson in view of Ishizuka et al., Levinson discloses that the controller IC is configured to receive from the host, by way of at least one of the pair of pins, at least one of the following: a command; data; and, diagnostic parameter information (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claims 7 and 22**, in the system described by Levinson in view of Ishizuka et al., Ishizuka et al. further teach a 2 x 10 pin arrangement (Figure 2A shows at least ten pins/contacts in each row, for example).

Regarding **claims 8 and 23**, Levinson disclose that the diagnostic parameter information includes at least status information (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 11**, Levinson discloses that the controller IC is configured to generate at least one of: a temperature dependent output; and, a temperature independent output, at least in the sense that Levinson discloses that the controller IC is configured to generate outputs, and any such outputs are inherently one of either "temperature dependent" or "temperature independent."

Regarding **claim 12**, Levinson discloses that the controller IC further comprises an analog monitoring connection (column 4, lines 19-68; column 1-18).

Regarding **claims 15, 35, and 36**, in the system described by Levinson in view of Ishizuka et al., the optical module is configured to transmit a "transmitter fault" signal to the host

by way of one of the pins of the pinout arrangement, wherein the "transmitter fault" signal is transmitted to the host by way of one of the pair of pins. Specifically, Levinson discloses outputting a signal indicating a transmitter fault to the host (column 9, lines 1-14), wherein the signal would be transmitted through a pin as already taught by Ishizuka et al.

Regarding **claim 16**, Levinson discloses a plurality of memory mapped locations (i.e., locations in EEPROM 166), at least one of which is accessible by way of the serial digital interface (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 27**, Levinson discloses that at least one of the plurality of memory mapped locations is configured to be read, and written to, by way of the serial digital interface (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 28**, Levinson discloses at least one of the memory mapped locations is configured to receive and store information including optical transmit power and laser temperature (column 4, lines 20-32; column 6, lines 40-45; column 9, lines 1-35; column 10, lines 57-66)

Regarding **claim 29**, Levinson discloses that the diagnostic parameter information stored in the at least one memory mapped location is in a digitized form (column 10, lines 28-66).

Regarding **claim 30**, in the system described by Levinson in view of Ishizuka et al., Ishizuka et al. further teach that the pin array comprises two rows of six pins each (Figure 2A shows a pin array having two rows of at least six pins each), each pin of the two rows of six pins comprising one of the following: a serial communication data pin; a receiver ground pin; a receiver power pin; a signal detect pin; a receive data inverted pin; a receive data pin; a serial communication clock pin; a transmitter power pin; a transmitter ground pin; a transmitter

disable pin; a transmit data pin; a transmit data inverted pin; an interrupt pin; and a loss of signal pin (column 8, Table 2).

Regarding **claim 31**, Levinson disclose elements including an electrothermal cooler 150, an analog-to-digital converter 170; and a digital-to analog converter 180.

Regarding **claim 37**, Levinson discloses a memory map table associated with at least one of the plurality of memory map locations comprises information indicating at least a storage location of a measured value of a diagnostic parameter (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 47**, in the system described by Levinson in view of Ishizuka et al., the pin array includes the pair of pins such that the pair of pins is used for multiple and different types of signals, at least one of which is digital parameter information. Specifically, Levinson discloses outputting different types of signals including digital parameter information (column 10, lines 28-66; column 15, lines 26-36), wherein the signals would be transmitted through the pins as already taught by Ishizuka et al.

Regarding **claim 48**, Levinson in view of Ishizuka et al. describe a system as discussed above with regard to claim 1, including a pin array having pins arranged in two rows (Ishizuka et al., Figure 2A shows two rows of pins), but they do not explicitly disclose that the pair of pins is not aligned with either of the two rows. However, it is well understood in the art that electronic and optoelectronic modules may have various physical arrangements of pins. Regarding claim 48, it would have been obvious to a person of ordinary skill in the art to provide a plurality of pins arranged in two rows and the pair of pins not aligned with either of the two rows, as an engineering design choice of a way to physically arrange the pins in the module described by

Levinson in view of Ishizuka et al. The claimed differences exist not as a result of an attempt by Applicant to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art.

Regarding **claim 49**, in the system described by Levinson in view of Ishizuka et al., Levinson discloses memory (including EEPROM 166); and a memory interface for allowing a host device to read from and write to memory mapped locations within the memory in accordance with commands received from a host device, wherein the memory interface allows the host device to read digital values corresponding to the diagnostic parameter information from the memory mapped locations through the pair of pins (column 10, lines 28-66; column 15, lines 26-36).

5. **Claims 3, 18, and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** as applied to claims 1 and 17 above, and further in view of **Keevill et al.** (US 6,359,938 B1).

Regarding **claims 3 and 18**, Levinson in view of Ishizuka et al. describe a system as discussed above with regard to claims 1 and 17 including a serial digital interface, but they do not specifically disclose I2C or MDIO serial communication. However, various serial interface standards are well known in the communications art. Keevill et al. in particular teach a system that is related to the one described by Levinson in view of Ishizuka et al. including a communications device 146 that communicates with a host device via a serial interface 142 (Figure 12). Keevill et al. further teach that the serial interface is compatible with I2C serial communication (Figure 55; column 37, lines 1-8). Regarding claims 3 and 18, it would have been obvious to a person of ordinary skill in the art to use a I2C serial communication standard

as taught by Keevill et al. in the system described by Levinson in view of Ishizuka et al. as an engineering design choice of a serial communication standard in order to allow the system to properly communicate with a particular host device as already disclosed by Levinson.

Regarding **claim 26**, Levinson in view of Ishizuka et al. describe a system as discussed above with regard to claims 17, including a plurality of memory mapped locations but does not specifically disclose registers. However, various types of memory elements, including registers, are well known in the electronic and communication arts, and Keevill et al. in particular teach using registers to store data values (column 7, lines 43-46). It would have been obvious to a person of ordinary skill in the art to specifically provide a register as taught by Keevill et al. in the system described by Levinson in view of Ishizuka et al. as an engineering design choice of a way to effective implement the storage element already disclosed and thereby store values for later retrieval.

6. **Claims 5, 9, 20, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** as applied to claims 1 and 17 above, and further in view of **Levy et al.** (US 6,317,804 B1).

Regarding **claims 5, 9, 20, and 24**, Levinson in view of Ishizuka et al. describe a system as discussed above with regard to claims 1 and 17, including a plurality of pins and pins connected to an interface. They do not specifically teach that one of the pins comprises a serial communication data pin configured to communicate with the host by way of an SDA interface line, and the other of the pair of pins comprises a serial communication clock pin configured to communicate with the host by way of an SCL interface line.

However, it is well understood in the communications art that a serial interface as already disclosed by Levinson includes more than one electrical contact/line to successfully provide bidirectional signals between the transceiver and host. In the system described by Levinson in view of Ishizuka et al. as discussed above, it would have been obvious to a person of ordinary skill in the art to provide the interface connection disclosed by Levinson through at least two of the pins as taught by Ishizuka et al. in order to enable the interface connection to extend from the protective housing and effectively connect to the host computer. Furthermore, Levy et al. teach a system that is related to the one described by Levinson in view of Ishizuka et al. including serial interfaces and further teach serial communication data and serial communication clock lines (column 5, lines 62-67; column 6, lines 1-8). Regarding claims 5, 9, 20, and 24, it would have been obvious to a person of ordinary skill in the art to include serial communication data out and SDA interface line; and serial communication clock and SCL interface line as taught by Levy et al. in the system described by Levinson in view of Ishizuka et al. in order to effectively enable synchronized communication between the transceiver and the host and ensure that signals are properly received by the host from the transceiver.

7. **Claims 6 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** as applied to claims 1 and 17 respectively above, and further in view of **Applicant's Admitted Prior Art.**

Regarding **claims 6 and 21**, Levinson in view of Ishizuka et al. describe a system as discussed above with regard to claims 1 and 17, respectively, including a pin array, but they do not specifically teach substantial conformity with the Small Form Factor (SFF) configuration standard.

However, it is well known in the communication and electronic arts that standards may be used to ensure that various components effectively connect to each other, and Applicant's Admitted Prior Art teaches that Small Form Factor optoelectronic transceivers conforming to the Small Form Factor configuration standard are well known in the art (Applicant's specification, page 5). Regarding claims 6 and 21, it would have been obvious to a person of ordinary skill in the art to have the transceiver described by Levinson in view of Ishizuka et al. substantially conform to the Small Form Factor configuration standard as taught by Applicant's Admitted Prior Art in order to advantageously enable the transceiver to properly connect to other components in a standardized way and effectively provide interchangeability of transceiver modules.

8. **Claims 10, 13, 14, 25, and 32-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** as applied to claims 1 and 17 above, and further in view of **SFF Committee** ("SFF-8053 Specification for GBIC (Gigabit Interface Converter) Rev. 5.5," September 27, 2000).

Regarding claims 10, 13, 14, 25, and 32-34, Levinson in view of Ishizuka et al. describe a system as discussed above with regard to claims 1 and 17 above, including pins, a host receiving signals from the optical module, and a serial digital interface.

Regarding **claims 10 and 25**, Levinson in view of Ishizuka et al. do not specifically disclose that the pair of pins is configured for repeated pluggability. However, SFF Committee teaches a system that is related to the one described by Levinson in view of Ishizuka et al. including an optoelectronic module and a pinout arrangement including pins arranged for communication with a host by way of a corresponding interface line (page 4, Figure 1; pages 12-

13, Table 8 and "5.2.1 Serial module definition protocol" and pages 44-52, "Annex D: Module definition '4' GBIC (Serial Identification)"). SFF Committee further teach that the pins are configured for repeated pluggability (pages 20-29, "6 Mechanical interface for all GBICs"). Regarding claims 10 and 25, it would have been obvious to a person of ordinary skill in the art to configure the pins for repeated pluggability as taught by SFF Committee in the system described by Levinson in view of Ishizuka et al. in order to advantageously ensure that the module will physically withstand insertion and removal from a larger overall system without experiencing damage and thereby enable the module to be changed or moved as desired by users.

Regarding **claim 13**, Levinson in view of Ishizuka et al. do not specifically disclose that the serial digital interface substantially conforms to one of: a GBIC standard; and, the SFF standard. However, SFF Committee further teaches in a related system a serial digital interface substantially conforming to a GBIC standard (pages 3-7, "3 Introduction and overview"; pages 44-52, "Annex D: Module definition '4' GBIC (Serial Identification)"). Regarding claim 13, it would have been obvious to a person of ordinary skill in the art to have the serial digital interface already described by Levinson in view of Ishizuka et al. substantially conform to a GBIC standard as taught by SFF Committee in order to advantageously enable the module to properly connect to other components of the overall system (such as host computers) in a standardized way and effectively provide interchangeability of elements.

Regarding **claims 14 and 32-34**, Levinson in view of Ishizuka et al. do not specifically disclose that module is configured to receive a "rate select" signal from the host by way of one of the pins of the pinout arrangement.

However, SFF Committee further teaches in a related system an optical module configured to receive a "rate select" signal from a host by way of one of a pair of pins in a pinout arrangement, wherein the "rate select" signal includes at least "high" and "low" values, each of which corresponds to a different data rate (pages 12-13, "5.2.1 Serial module definition protocol" and pages 44-52, "Annex D: Module definition '4' GBIC (Serial Identification)"). Regarding claims 14 and 32-34, it would have been obvious to a person of ordinary skill in the art to include a "rate select" select as taught by SFF Committee in the system described by Levinson in view of Ishizuka et al. in order to advantageously enable a user to adjust the communication rate of the optoelectronic module via the host computer and thereby transmit/receive signals having different rates as desired to properly communicate with other optical devices in the overall system/network.

9. **Claims 38, 39, 41, 43, 44, 46, and 50-52** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** and **Applicant's Admitted Prior Art.**

Regarding **claim 38**, Levinson discloses an optoelectronic module (Figure 3), comprising:

an optoelectronic component (e.g., laser diode 100 or photo diode 224);

a controller IC (including microcontroller 162) including a serial digital interface (i.e., RS232 I/O port 200) configured to facilitate communication, between the optoelectronic module and a host (i.e., computer 202), of diagnostic parameter information concerning the optoelectronic component.

Regarding claim 38, Levinson does not specifically disclose positioning the elements of the transceiver system in a housing and does not specifically disclose a pinout arrangement

comprising: a pin array having a plurality of pins in communication with the controller and a pair of pins in communication with the interface.

However, it is well understood in the art that a transceiver system such as disclosed by Levinson may be placed in a housing in order to protect the various components from damage. Ishizuka et al. teach a system that is related to the one described by Levinson, including an optical transmitter 201, an optical receiver 202, and controller elements including circuit 203 (Figures 2A-C). Ishizuka et al. further teach disposing the transceiver elements in a housing 405 and further teach a pin array (i.e., lead terminals 404).

Examiner notes that Ishizuka et al. particularly teach that the pins and electrical contacts are used to enable the transceiver components within the housing to further connect to and communicate with additional elements outside of the housing in the context of an overall communication system (column 6, lines 21-32 and column 8, Table 2).

Regarding claim 38, it would have been obvious to a person of ordinary skill in the art to provide a housing as taught by Ishizuka et al. in the system disclosed by Levinson in order to advantageously protect the optoelectronic elements from damage while enabling the elements to transmit and receiver optical signals and connect to other elements of the communication system. It further would have been obvious to a person of ordinary skill in the art to provide a pin array and pins as taught by Ishizuka et al. in the system disclosed by Levinson in order to advantageously enable the components of the optical transceiver to physically connect to other elements through the housing. Examiner notes that Levinson already discloses that the transceiver includes an interface (RS232 I/O port 200) that is connected to a host computer. In the system described by Levinson in view of Ishizuka et al. as discussed above, it would have

been obvious to a person of ordinary skill in the art to provide the interface connection disclosed by Levinson through pins as taught by Ishizuka et al. in order to enable the interface connection to extend from the protective housing and effectively connect to the host computer.

Further regarding claim 38, Levinson in view of Ishizuka do not specifically teach substantial conformity with the Small Form Factor (SFF) configuration standard.

However, it is well known in the communication and electronic arts that standards may be used to ensure that various components effectively connect to each other, and Applicant's Admitted Prior Art teaches that Small Form Factor optoelectronic transceivers conforming to the Small Form Factor configuration standard are well known in the art (Applicant's specification, page 5). Regarding claim 38, it would have been obvious to a person of ordinary skill in the art to have the transceiver described by Levinson in view of Ishizuka et al. substantially conform to the Small Form Factor configuration standard as taught by Applicant's Admitted Prior Art in order to advantageously enable the transceiver to properly connect to other components in a standardized way and effectively provide interchangeability of transceiver modules.

Regarding **claim 39**, Levinson discloses that the optoelectronic component comprises at least one of: a transmit optical subassembly (i.e., laser diode 100); and, a receive optical subassembly (i.e., photo diode 224).

Regarding **claim 41**, in the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art, Levinson discloses that the controller IC is configured to receive from the host, by way of at least one of the pair of pins, at least one of the following: a command; data; and, diagnostic parameter information (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 43**, in the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art, Ishizuka et al. further teach a 2 x 10 pin arrangement (Figure 2A shows at least ten pins/contacts in each row, for example).

Regarding **claim 44**, Levinson disclose that the diagnostic parameter information includes at least a measured value of a diagnostic parameter (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 46**, Levinson discloses a plurality of memory mapped locations (i.e., locations in EEPROM 166), at least one of which is accessible by way of the serial digital interface and which is configured to receive and store information concerning at least one diagnostic parameter (column 10, lines 28-66; column 15, lines 26-36).

Regarding **claim 50**, in the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art, the pin array includes the pair of pins such that the pair of pins is used for multiple and different types of signals, at least one of which is digital parameter information. Specifically, Levinson discloses outputting different types of signals including digital parameter information (column 10, lines 28-66; column 15, lines 26-36), wherein the signals would be transmitted through the pins as already taught by Ishizuka et al.

Regarding **claim 51**, Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art describe a system as discussed above with regard to claim 38, including a pin array having pins arranged in two rows (Ishizuka et al., Figure 2A shows two rows of pins), but they do not explicitly disclose that the pair of pins is not aligned with either of the two rows. However, it is well understood in the art that electronic and optoelectronic modules may have various physical arrangements of pins. Regarding claim 51, it would have been obvious to a person of ordinary

skill in the art to provide a plurality of pins arranged in two rows and the pair of pins not aligned with either of the two rows, as an engineering design choice of a way to physically arrange the pins in the module described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art. The claimed differences exist not as a result of an attempt by Applicant to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art.

Regarding **claim 52**, in the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art, Levinson discloses memory (including EEPROM 166); and a memory interface for allowing a host device to read from and write to memory mapped locations within the memory in accordance with commands received from a host device, wherein the memory interface allows the host device to read digital values corresponding to the diagnostic parameter information from the memory mapped locations through the pair of pins (column 10, lines 28-66; column 15, lines 26-36).

10. **Claim 40** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** and **Applicant's Admitted Prior Art** as applied to claim 38 above, and further in view of **Keevill et al.**

Regarding **claim 40**, Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art describe a system as discussed above with regard to claims 1 and 17 including a serial digital interface, but they do not specifically disclose I2C or MDIO serial communication. However, various serial interface standards are well known in the communications art. Keevill et al. in particular teach a system that is related to the one described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art including a communications device 146 that

communicates with a host device via a serial interface 142 (Figure 12). Keevill et al. further teach that the serial interface is compatible with I2C serial communication (Figure 55; column 37, lines 1-8). Regarding claim 40, it would have been obvious to a person of ordinary skill in the art to use a I2C serial communication standard as taught by Keevill et al. in the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art as an engineering design choice of a serial communication standard in order to allow the system to properly communicate with a particular host device as already disclosed by Levinson.

11. **Claims 42 and 45** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Levinson** in view of **Ishizuka et al.** and **Applicant's Admitted Prior Art** as applied to claim 38 above, and further in view of **Levy et al.**

Regarding **claims 42 and 45**, Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art describe a system as discussed above with regard to claim 38, including a plurality of pins and pins connected to an interface. They do not specifically teach that one of the pins comprises a serial communication data pin configured to communicate with the host by way of an SDA interface line, and the other of the pair of pins comprises a serial communication clock pin configured to communicate with the host by way of an SCL interface line.

However, it is well understood in the communications art that a serial interface as already disclosed by Levinson includes more than one electrical contact/line to successfully provide bidirectional signals between the transceiver and host. In the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art as discussed above, it would have been obvious to a person of ordinary skill in the art to provide the interface connection disclosed by Levinson through at least two of the pins as taught by Ishizuka et al. in order to enable the

interface connection to extend from the protective housing and effectively connect to the host computer. Furthermore, Levy et al. teach a system that is related to the one described by Levinson in view of Ishizuka et al. including serial interfaces and further teach serial communication data and serial communication clock lines (column 5, lines 62-67; column 6, lines 1-8). Regarding claims 42 and 45, it would have been obvious to a person of ordinary skill in the art to include serial communication data out and SDA interface line; and serial communication clock and SCL interface line as taught by Levy et al. in the system described by Levinson in view of Ishizuka et al. and Applicant's Admitted Prior Art in order to effectively enable synchronized communication between the transceiver and the host and ensure that signals are properly received by the host from the transceiver.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re*

Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. **Claim 53** is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 62 of U.S. Patent No. 7,079,775 B2, claim 1 of U.S. Patent No. 6,941,077 B2, claim 1 of U.S. Patent No. 6,952,531 B2, claim 1 of U.S. Patent No. 6,957,021 B2, claim 32 of U.S. Patent No. 7,058,310 B2,** or **claim 37 of U.S. Patent No. 7,184,668 B2,** each separately in view of **Ishizuka et al.** (US 5,479,288 A).

Claim 53 of the present application and claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, claim 32 of US 7,058,310 B2, and claim 37 of US 7,184,668 B2 each recite circuitry for an optoelectronic device including analog to digital conversion circuitry for receiving a plurality of analog signals from the optoelectronic device corresponding to operating conditions of the device, converting the received analog signals into digital values, and storing the digital values in predefined locations within a memory; and an interface configured to enable a host to read from host-specified

locations within the memory. Further regarding claim 53 of the present application, claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, claim 32 of US 7,058,310 B2, and claim 37 of US 7,184,668 B2 and claim 14 each further recite comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined locations within the memory during operation of the optoelectronic transceiver.

Claim 53 of the present application and claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, claim 32 of US 7,058,310 B2, and claim 37 of US 7,184,668 B2 also each further recite an optoelectronic component or optical transmitter/receiver.

Claim 53 of the present application and claim 37 of US 7,184,668 B2 also each further recite a housing.

Further regarding claim 53 of the present application, claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, and claim 32 of US 7,058,310 B2 do not specifically recite positioning the elements of the transceiver system in a housing. Claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, claim 32 of US 7,058,310 B2, and claim 37 of US 7,184,668 B2 also do not specifically recite a pinout arrangement comprising a pin array and a pair of pairs in communication with the interface.

However, it is well understood in the art that an optoelectronic device may be placed in a housing in order to protect the various components from damage. Ishizuka et al. teach an optical transmitter 201, an optical receiver 202, and controller elements including circuit 203 (Figures

2A-C). Ishizuka et al. further teach disposing the transceiver elements in a housing 405 and and further teach a pin array (i.e., lead terminals 404). Examiner notes that Ishizuka et al. particularly teach that the pins are used to enable the transceiver components within the housing to further connect to and communicate with additional elements outside of the housing in the context of an overall communication system (column 6, lines 21-32 and column 8, Table 2).

Regarding claim 53, given claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, or claim 32 of US 7,058,310 B2, it would have been obvious to a person of ordinary skill in the art to further provide a housing as taught by Ishizuka et al. in order to advantageously protect the optoelectronic elements from damage while enabling the elements to transmit and receiver optical signals and connect to other elements of the communication system.

Further regarding claim 53, given claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, claim 32 of US 7,058,310 B2, or claim 37 of US 7,184,668 B2, it also would have been obvious to a person of ordinary skill in the art to provide a pinout arrangement and pin array as taught by Ishizuka et al. in order to advantageously enable the components of the optical transceiver to physically connect to other elements through the housing. Examiner notes that claim 62 of US 7,079,775 B2, claim 1 of US 6,941,077 B2, claim 1 of US 6,952,531 B2, claim 1 of US 6,957,021 B2, claim 32 of US 7,058,310 B2, and claim 37 of US 7,184,668 B2 each already recite an interface that is connected to a host. It would have been obvious to a person of ordinary skill in the art to provide the interface connection through pins as taught by Ishizuka et al. in order to enable the interface connection to extend from the protective housing and effectively connect to the host.

Allowable Subject Matter

14. **Claim 53** may contain allowable subject matter but is currently rejected on the ground of nonstatutory obviousness-type double patenting as discussed in detail above and is not currently allowed.

15. The following is a statement of reasons for the indication of allowable subject matter: The prior art, including Levinson and Ishizuka et al., does not specifically disclose or fairly suggest an optoelectronic module including the particular combination of all of the elements and limitations recited in claim 53, particularly including comparison logic configured to compare the recited digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory-mapped flag storage locations during operation of an optoelectronic component; and a serial digital interface configured to enable a host to read from host-specified memory-mapped locations, including the predefined memory-mapped flag storage locations

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung, whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christina Y. Leung/

Primary Examiner, Art Unit 2613